**EEL 4914 Senior Design I**

**Divide and Conquer Guideline**

The Divide and Conquer document acts as the proposal of your Senior Design project. It should be at least 10-page long and contain all, but not limited to, the following content.

**Cover Page**

* + descriptive title of the project
  + group number
  + group members’ names
  + group members’ degree majors
  + reviewers, advisors, sponsors, customers or significant contributors

**Content** (at least 10 pages)

* + motivation and background

Our senior design group is tasked with designing an Application-Specific Integrated Circuit (ASIC), specifically focused on the design and synthesis of a RISC32I Central Processing Unit (CPU) core. A complete CPU comprises several computational units, along with various interconnects to external hardware such as RAM and PCIe devices. Our project zeroes in on the core computational unit of the CPU, which is responsible for executing the user’s instructions—ranging from logic and arithmetic operations to memory read/write functions. These fundamental tasks lie at the heart of modern digital computing.

Our CPU core will implement the RISC32I Instruction Set Architecture (ISA), which defines the interface between software and hardware. The RISC32I ISA is an open-source standard that already has established compiler support. This is a key advantage, as it allows us to leverage existing tools such as operating systems, compilers, linkers, APIs, and software. By utilizing a well-supported ISA, we sidestep one of the primary challenges to adopting new CPU architectures: the availability of toolchain support. A powerful CPU architecture can be held back if the necessary development tools—compilers, debuggers, and other software—are not readily available. Our choice of the RISC32I ISA ensures that we can tap into a robust ecosystem of existing technologies, facilitating a smoother development process and increasing the potential for adoption.

Semiconductor fabrication and design are integral to the United States' economic stability, national security, and supply chain resilience. A disruption in the steady supply of chips can have significant consequences, as demonstrated by the global semiconductor shortage triggered by the COVID-19 pandemic in 2020. Industries ranging from defense to automotive manufacturing experienced substantial setbacks due to port closures in key production regions. This disruption highlighted the dependency of modern industries on a reliable supply of chips. For example, the automotive sector faced production halts as critical components became unavailable, and the defense industry experienced delays in both maintenance and production of essential equipment. This project aims to address such vulnerabilities by advancing the design of Application-Specific Integrated Circuits (ASICs), contributing to a more secure and self-sustaining semiconductor ecosystem.

To help create a more robust semiconductor Industry in the Unitied States, this project will help train and provide industry-level experience of ASIC design to UCF students in order to create a larger pool of ASIC talent here in the United States. The project will help create a pipeline of UCF students to continue in ASIC design.

* + goals and objectives/design requirements including basic, advance and stretch goals
  + description of features/functionalities
    - * + reference any input from customers or marketing analysis of comparable products/projects that has been used to identify project features
  + existing product/past project/prior related work
  + table of at least 7 key engineering specifications with quantitative measures
    - highlight 3 demonstrable specifications
  + detailed hardware block diagram (at least one)
    - use color blocks to indicate work distribution
    - indicate both the input and output of each block
    - illustrate clearly the external inputs and outputs of your system
    - indicate the status of each block (to be acquired, acquired, investigating, designing, prototyping, completed)
    - legend (if applicable)
    - include as much detail as possible to facilitate clear understanding of the diagram
  + detailed software diagram/flowchart (at least one)
    - use color blocks to indicate work distribution
    - indicate both the input and output of each block
    - legend (if applicable)
    - include as much detail as possible to facilitate clear understanding of the diagram
  + prototype illustration (if applicable)
  + house of quality
  + budget and financing
  + project milestones for SD1 and SD2

**NOTE:** The above sequence of items does not necessarily indicate the order of content of your report. To produce a well-written report, you need to organize the content in a way that allows the passages to flow, paragraphs to be coherently interconnected, and ideas to be logically connected from one to another, so that your readers can easily grasp and understand the overall pictures and details of your project.

**Appendices**

* + **Appendix A** – reference
  + **Appendix B** – copyright permission
  + **Appendix C** – etc.

**NOTE:** The answer to the question “Do I need to cite this material?” is always a

'YES’. The reason is simple. It is always better to provide proper citation than

not. So, please contact the authors/creators/producers to request for permission to use

their material. All requests and approvals should be documented in this section. For

all requests that have been rejected, the corresponding materials MUST be removed

from the final document.